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09/008,531	01/16/1998	HOWARD E. RHODES	MIO012V2	6336

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EXAMINER	
TRINH, MICHAEL MANH	

ART UNIT	PAPER NUMBER
2822	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/008,531	RHODES, HOWARD E.	
	Examiner	Art Unit	
	Michael Trinh	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-25,31 and 32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-25,31 and 32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

*** This office action is in response to Applicant's Brief filed July 29, 2004. Claims 21-25 and 31-32 are pending.

*** The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 102

1. Claims 21,22,23,25 are rejected under 35 U.S.C. 102(e) as being anticipated by Jost et al (5,563,089).

Jost et al '089 teach (at Figs 10-12; col 5, line 37 through col 6) a method for forming a semiconductor device comprising at least the steps of: providing a substrate 11 having at least one semiconductor substrate layer 11 or polysilicon gates 12,14,16 (Fig 10; Fig 1, col 3, lines 37-50); forming an underlayer 28 having an opening over the at least one semiconductor layer; forming a layer 40 of conductive material over the underlayer 28 and in the opening, the layer 40 of conductive material having a topography that includes a substantially vertical component in the opening of the underlayer 28 (Fig 10; col 5,lines 37-65; and Figs 1-6, col 3, line 38 through col 5); forming an overlayer 44a over the layer 40 of conductive material (Fig 10); etching a contact hole in the overlayer 44a and in an overetch amount of the substantially vertical component of the layer 40 of conductive material in the opening (Fig 11; col 5, lines 51-65; Figs 6-7, col 5, lines 6-26); and forming a contact 46a in the contact hole disposed adjacent to and directly contacting the vertical component (Fig 12). Re claim 22, wherein the vertical component in the opening of the underlayer 28 defines a localized thick region in the layer 40 of conductive material (Figs 10-12). Re claim 23, wherein the vertical component in the layer 40 of conductive material in the opening of the underlayer 28 is a spacer as shown in Figures 10-12. Re claim 25, wherein the conductive layer 40 is a capacitor electrode (Figs 10-12; Figs 5-8; col 4, line 58 through col 5, line 65).

2. Claims 21-25,31,32 are rejected under 35 U.S.C. 102(e) as being anticipated by Jun (5,459,094).

Re claim 21, Jun teaches (at Figures 4a-4f;8a-8f) a method for forming a semiconductor device comprising at least the steps of: providing a substrate 100 having at least one

semiconductor layer (100 or 13; Figs 4a, col 4, lines 45-63, Fig 8a-8f; col 10, line 6 through col 11, line 15) forming an underlayer 14 of a structure having an opening 15 over the at least one semiconductor layer 100/13 (Figs 4a,8a; col 5, lines 1-14); forming a layer 16 of conductive material over the under layer and in the opening 15, the layer of conductive material having a topography that includes a substantially vertical component in the opening (Figs 4b,8b; col 5, lines 15-25); forming an overlayer (17 in Fig 4b-4c; 25 in Figs 8b-8c) over the layer 16 of conductive material; etching a contact hole in the overlayer and in an overetch amount of the substantially vertical component of the layer 16 of conductive material in the opening (Fig 4c;8c; col 5, lines 31-57; col 11, lines 44-55); and forming a contact 19 in the contact hole disposed adjacent to and directly contacting the vertical component (Fig 4e; col 5, line 58 through col 6; Fig 8d-f; col 10, line 59 through col 11). Re claim 22, wherein the vertical component defines a localized thick region in the layer 16 of conductive material (Figs 4a-4f;8a-8f). Re claim 23, wherein the vertical component of the layer 16 of conductive material is a spacer located in the contact hole 15 of the underlayer 14 (Figs 4f,8f). Re claim 24, the method further comprises forming a structure 14 having an opening therein under the conductive layer 16 and filling the opening 14 with the conductive material 16 to form the vertical component (Figs 4a-4f;8a-8f). Re claim 25, wherein the conductive layer 16 is a capacitor electrode (Figs 4a-4f,8a-8f; col 6, lines 15-27). Re claim 21, Jun teaches (at Figures 4a-4f;8a-8f) a method for forming a semiconductor device comprising at least the steps of: providing a substrate 100 having at least one semiconductor layer (13; Figs 4a, col 4, lines 45-63, Fig 8a-8f; col 10, line 6 through col 11, line 15) forming an underlayer 14 of a structure having an opening 15 in the at least one semiconductor layer 13 (Figs 4a,8a; col 5, lines 1-14); forming a layer 16 of conductive material over the at least one semiconductive layer 13, and filling the opening 15 with the layer 16 of conductive material to form a substantially vertical component in the opening (Figs 4b,8b; col 5, lines 15-25); forming an overlayer (17 in Fig 4b-4c; 25 in Figs 8b-8c) over the layer 16 of conductive material; forming a contact hole in the overlayer and extending into the vertical component of the layer 16 of conductive material in the opening (Fig 4c;8c; col 5, lines 31-57; col 11, lines 44-55), the contact hole disposed adjacent to and directly contacting the vertical component in the opening; and filling the contact hole with a conductive material 19 (Fig 4e; col 5, line 58 through col 6; Fig 8d-f; col 10, line 59 through col 11). Re claim 32, wherein the

vertical component defines a localized thick region in the layer 16 of conductive material (Figs 4a-4f;8a-8f).

Claim Rejections - 35 USC § 103

3. Claims 21-22,24,31,32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bergemont (5,484,741) taken with Toshiyuki et al (JP-05-109905) and Zamanian (5,793,111).

Re claim 21, Bergemont teaches (at least from Figures 9-14; col 7, line 25 through col 10) a method for forming a semiconductor device comprising at least the steps of: providing a semiconductor substrate 102 having at least one semiconductor layer 102 (col 7, line 17 through col 8); forming an underlayer 118 having an opening over the at least one semiconductor layer 102 (Figs 12,11,13; col 8, lines 44 through col 9, line 22, in which the underlayer is the remaining portion of the second oxide underlayer 118 located above the "Source" after removing the photoresist 120, see Figs 12-13,11); forming a layer 122 of conductive material over the underlayer 118 and in the opening (Figs 11-13, after removing photoresist 120), the layer 122 of conductive material having a topography that includes a substantially vertical component in the opening (Fig 13, opening located above the "Source" and "CSBL"; col 9, lines 23-53); forming an overlayer 124 over the layer of conductive material 122 (Fig 14; col 9, lines 54-59); etching a contact hole in the overlayer 124 to expose the substantially vertical component of the layer of conductive material 122 in the opening (Fig 14; col 9, lines 60-67); and forming a contact 126 in the contact hole disposed adjacent to and directly contacting the vertical component. Re claim 22, wherein the vertical component defines a localized thick region in the layer 122 of conductive material (as shown in Figs 13-14). Re claim 24, the method further comprises forming the structure of the underlayer 118 having an opening therein (Fig 13, the underlayer is the portion of the second oxide 118 after removing the photoresist 120 in Fig 12, which underlayer is located above the "Source") under the conductive layer 122 and filling the opening with the conductive material 122 to form the vertical component (Fig 13). Re further claim 31, Bergemont teaches (at least from Figures 9-14; col 7, line 25 through col 10) a method for forming a semiconductor device comprising at least the steps of: providing a semiconductor substrate 102 having at least one semiconductor layer (col 7, line 25 through col 8); forming an underlayer 118 comprising a structure having an opening in the at least one semiconductor layer 106 (Figs 12,13,11; col 8, lines 44 through col 9, line 22, wherein the structure is the remaining

portion of the second oxide underlayer 118 located above the "Source", after removing the photoresist 120, shown in Figs 12-13,11); forming a layer 122 of conductive material over the at least one semiconductor layer 106, and filling the opening with the conductive material 122 to form a substantially vertical component (Fig 13, opening in the structure located above the "Source" and "CSBL"; col 9, lines 23-53); forming an overlayer 124 over the layer of conductive material 122 (Fig 14; col 9, lines 54-59); forming a contact hole in the overlayer 124 to expose the substantially vertical component of the layer of conductive material 122, the contact hole disposed adjacent to and directly contacting the vertical component in the opening (Fig 14; col 9, lines 60-67); and filling the contact hole with a conductive material to form a contact 126 in the contact hole disposed adjacent to and directly contacting the vertical component. Re claim 32, wherein the vertical component defines a localized thick region in the layer 122 of conductive material located above the "Source" and "CSBL" (as shown in Figs 13-14).

Re claims 21 and 31, Bergemont lacks showing the etching in an overetch amount of the substantially vertical component of the layer 122 of the conductive material ("extending into..." as in claim 31).

However, Toshiyuki et al (JP-05-109905) teaches (at Figs 1-4; English abstract and Computer-English Translation pages 1-3) forming a layer of conductive material 2 over an underlayer (Fig 2); forming an overlayer 3 over said layer of conductive material (Fig 2); etching to form a contact hole 9 in the overlayer 3 and in an overetch amount of the layer of the conductive material having a vertical component (Fig 3,1); and forming a contact 6,8 (Figs 1,4) in said contact hole 9 disposed adjacent to and directly contacting the substantially vertical component, in the layer of conductive material, and contacting the layer of conductive material 2. Zamanian also teaches (at Fig 6,1-5; col 5, line 50 through col 6, lines 22; cols 3-5) that in order to insure that all of the dielectric has been removed from the contact opening, etching a contact hole in the overlayer 40 and in an overetch amount of the layer of conductive material having a substantially vertical component.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the contact hole of Bergemont by etching a contact hole in the overlayer 124 and in an overetch amount and extending into the layer 122 of conductive material having a

substantially vertical component, as taught by Toshiyuki and Zamanian. This is because of the desirability to improve reliability in the multilayer interconnection structure, and to suppress occupied area of a contact part between top and bottom wiring patterns. This is also because of the desirability to insure that all of the dielectric of the overlayer has been completely removed from the contact hole for providing a secure and good electrical connection from the layer of conductive material to the contact.

4. Claims 21-25,31-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuo et al (5,312,769) taken with Zamanian (5,793,111) and Toshiyuki et al (JP-05-109905).

In re claims 21, and 31, Matsuo shows in Figures 2A-2E and related text, a process for making a semiconductor device including the steps of providing a substrate having at least one semiconductor layer 1 and with semiconductor gate electrode layers having opening including sidewalls formed thereon; forming an underlayer structure 21 having an opening over and in the at least one semiconductor layer 102; forming over the underlayer structure and filling the opening with a layer of conductive material 12 having a topography that includes a substantially vertical component defining a localized thick region; forming an overlayer over said layer of conductive material; forming contact hole in the overlayer and in an overetch amount of the substantially vertical component; and forming a contact in said contact hole disposed adjacent to and directly contacting the substantially vertical component. Matsuo also shows wherein the contact hole window 29 is formed in the first interlayer insulating film 23 formed by using a dry etching technique (see Figure 2B; column 5, lines 30-46). Matsuo further shows in Figure 2B wherein the overlayer is made of oxide material and wherein the layer of conductive material is made of polysilicon (col 3, line 59 through col 5, line 55). Re claims 22 and 32, Matsuo et al shows the vertical component defining a localized thick region in the layer 12 of conductive material. Re claim 23, Matsuo shows wherein the vertical component of the layer 12 of conductive material is a spacer (Figs 2b,2c). Re claim 24, Matsuo forms a structure 21 having an opening therein under the conductive layer 12 and filling the opening with the conductive material to form the vertical component (Figs 2a-2c). Re claim 25, Matsuo shows wherein the contact 13 disposed adjacent to and contacting the vertical component 12 is a storage capacitor

electrode made of the same material as the layer of conductive material (column 4, lines 3-22), in which the layer of conductive material is considered a part of the capacitor electrode.

Matsuo fails to show etching in an overetch amount of the substantially vertical component.

However, Zamanian teaches (at Fig 6,1-5; col 5, line 50 through col 6, lines 22; cols 3-5) that in order to insure that all of the dielectric has been removed from the contact opening, etching a contact hole in the overlayer 40 and in an overetch amount of the layer of conductive material having a substantially vertical component. Toshiyuki et al (JP-05-109905) teaches (at Figs 1-4; English abstract and Computer-English Translation pages 1-3) forming a layer of conductive material 2 over an underlayer (Fig 2); forming an overlayer 3 over said layer of conductive material (Fig 2); etching to form a contact hole 9 in the overlayer 3 and in an overetch amount of the layer of the conductive material having a vertical component (Fig 3,1); and forming a contact 6,8 (Figs 1,4) in said contact hole 9 disposed adjacent to and directly contacting the substantially vertical component, in the layer of conductive material, and contacting the layer of conductive material 2.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the contact hole of Matsuo et al (Figure 2B) by etching a contact hole in the overlayer insulator 23 and in an overetch amount of the layer 12 of conductive material having a substantially vertical component, as taught by Zamanian and Toshiyuki, wherein the contact is formed in the overlayer and in said vertical component. This is because of the desirability to insure that all of the dielectric of the overlayer has been completely removed from the contact hole for providing a secure and good electrical connection from the layer of conductive material to the contact. This is also because of the desirability to improve reliability in the multilayer interconnection structure, and to suppress occupied area of a contact part between top and bottom wiring patterns.

Response to Argument

*** In view of new ground(s) of rejections, rejections using Zamanian (5,793,111) and Okada et al (5,399,890) as primary references are withdrawn since they are as cumulative.

*** Applicant's remarks in the Brief filed on July 29, 2004 have been considered but they are also in moot of new ground of rejections.

*** Claimed subject matter, not the specification, is the measure of invention. Limitations in the specification cannot be read into the claims for the purpose of avoiding the prior art. In Re Self, 213 USPQ 1,5 (CCPA 1982); In Re Priest, 199 USPQ 11,15 (CCPA 1978).

*** Regarding 35 USC 103 rejection using Matsuo as a main reference:

Applicant apparently remarked that "...no motivation to use the technique of Toshiyuki [and Zamanian]..." to etch a portion of the layer of conductive material in the contact hole.

In response, this is noted and found unconvincing. Toshiyuki and Zamanian clearly teaches over-etching of the underlying layer of conductive material (Fig 6) during formation of the contact hole. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the contact hole of Matsuo et al (Figure 2B) by etching a contact hole in the overlayer insulator 23 and in an overetch amount of the layer 12 of conductive material having a substantially vertical component, as taught by Zamanian and Toshiyuki, wherein the contact is formed in the overlayer and in said vertical component. This is because of the desirability to insure that all of the dielectric of the overlayer has been completely removed from the contact hole for providing a secure and good electrical connection from the layer of conductive material to the contact. This is also because of the desirability to improve reliability in the multilayer interconnection structure, and to suppress occupied area of a contact part between top and bottom wiring patterns.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F: 8:30 Am to 5:00 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the receptionist whose telephone number is (703) 308-0956.

Oacs-7&16

M. Trinh

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